전북대학교 강의계획서 (2024년 2학기)

교과목명	반도체공정	분반	1	담당교수명	에런스노버거
		학점	3	연락처	
교과목 코드	0000125132	요일/시간	월 8-A,월 8-B,월 9-A,월 9-B,수 8-A,수 8-B	E-mail	aaronkr.trainer@gmail.com
교과목 구분	전공선택			연구실	
학과/학년	국제이공학부(엔지니어링사이언스) 3	강의실	전주:인문대학2호관 501	상담가능시간	

1. 강의 기본정보

수업목표	Purpose of this course: (i) Overall concept of semiconductor material (ii) Concept of Crystals and Crystallographic Orientations (iii) Introduction of Microelectronic Fabrication, Thin Film Deposition process
직전강의평가 및 CQI반영사항	N/A

6대 핵심역량과의 관계

구분	소통역량	창의역량	인성역량	실무역량	도전역량	문화역량	합계	대표역량
비율(%)	20	10	20	20	20	10	100	

교과목간의 연계성					
주교재	Semiconductor Microchips and Fabrication: A Practical Guide to Theory and Manufacturing				
저자	Lian, Yaguang	출판사	Wiley-IEEE Press	출판년도	2023
참고자료					
교재언어	영어	강의언어	영어	필요 기자재	
권장 선수과목		권장 후수과목	DA		

수업방식 (복수가능√)	강의	발표/토론	PBL	플립러닝	LMS활용	실험실습	기타
	√	√					
수업운영방향							

평가계획 (100%)	중간	기말	출석	과제물	안전교육	발표/토론	수업태도	기타
	25%	35%	15%	15%	0%	10%	0%	0%
평가참고사항								

평가방법	절대평가	상대평가 비율	A(%)	A+B(%)	C이하(%)	총비율
			0	0	0	100%
		절대평가 기준	국제이공학부 절대평가 기준에 따름			

참고 사항

*** 장애학생 교수학습지원 사항**

- 강의 √ **강의 파일, 자료 등 제공** 좌석배치(지정좌석) 조정
  기타 : ---
- 과제 과제 제출기한 연장 √ **대안적 과제 제시**
- 평가 시험시간 연장 √ **평가방법 조정(대독, 구두응답, 도우미 대필 답안작성 등)**
  별도의 시험 장소 제공
  기타 : ---

그 외(필요시 자유로이 추가 기술) : ---

※ 위 지원사항 등을 포함한 강의, 과제, 시험 등 학습과정에서 장애로 인하여 추가 지원이 필요한 경우 개강전 담당강사 및 장애학습 지원센터를 통해 문의 바랍니다.

주별 강의내용

주별	수업목표	수업내용	수업방식	자료, 과제 및 기타 참고사항	수업방식별시간	
					온라인	오프라인
1주	Course Introduction 1 Intro to Basic Concepts	1.1 What Is a Microchip? 1 1.2 Ohm's Law and Resistivity 1 1.3 Conductor, Insulator, and Semiconductor 5	Lecture			

주별 강의내용						
주별	수업목표	수업내용	수업방식	자료, 과제 및 기타 참고사항	수업방식별시간	
					온라인	오프라인
2주	2 Intro of Theories 3 Early Radio Communication	2.1 The Birth of Quantum Mechanics 7 2.2 Energy Band (Band) 11 3.1 Telegraph Technology 17 3.2 Electron Tube 19	Lecture			
3주	4 Basic Knowledge of Electric Circuits 5 Discussion of Semiconductors & Diodes	4.1 Electric Circuits and the Components 23 4.2 Electric Field 26 4.3 Magnetic Field 28 4.4 Alternating Current 30 5.1 Semiconductor Energy Band 33 5.2 Semiconductor Doping 36 5.3 Semiconductor Diode 42	Lecture			
4주	6 Transistor & Integrated Circuit 7 Development History of Semiconductor Industry	6.1 Bipolar Transistor 47 6.2 Junction Field Effect Transistor 49 6.3 Metal-Semiconductor Field Effect Transistor 52 6.4 Metal-Insulator-Semiconductor Field Effect Transistor 55 7.1 The Instruction of Semiconductor Products and Structures 61 7.2 A Brief History of the Semiconductor Industry 63 7.3 Changes in the Size of Transistors and SiliconWafers 65 7.4 Clean Room 67 7.5 Planar Process 71	Lecture			
5주	8 Semiconductor Photonic Devices 9 Semiconductor Light Detection & Photocell	8.1 Light-Emitting Devices and Light-Emitting Principles 77 8.2 Light-Emitting Diode (LED) 82 8.3 Semiconductor Diode Laser 88 8.3.1 Resonant Cavity 89 8.3.2 Reflection and Refraction of Light 91 8.3.3 Heterojunction Materials 93 8.3.4 Population Inversion and Threshold Current Density 94 9.1 Digital Camera and CCD 97 9.2 Photoconductor 100 9.3 Transistor Laser 101 9.4 Solar Cell 105	Lecture			
6주	10 Manufacture of Silicon Wafer	10.1 From Quartzite Ore to Polysilicon 110 10.2 Chemical Reaction 113 10.3 Pull Single Crystal 115 10.4 Polishing and Slicing 116	Lecture			
7주	11 Basic Knowledge of Process	11.1 The Structure of Integrated Circuit (IC) 125 11.2 Resolution of Optical System 128 11.3 Why Plasma Used in the Process 131	Lecture			
8주	Midterm Examination	Written	Written Examination			
9주	12 Photolithography (Lithography)	12.1 The Steps of Lithography Process 135 12.1.1 Cleaning 135 12.1.2 Dehydration Bake 136 12.1.3 Photoresist Coating 138 12.1.4 Soft Bake 141 12.1.5 Alignment and Exposure 141 12.1.6 Developing 145 12.1.7 Inspection 146 12.1.8 Hard Bake 147 12.1.9 Descum 148 12.2 Alignment Mark (Mark) Design on the Photomask 152 12.3 Contemporary Photolithography Equipment Technologies 156	Lecture			
10주	13 Dielectric Films Growth 14 Intro to Etching and RIE System	13.1 The Growth of Silicon Dioxide Film 162 13.1.1 Thermal Oxidation Process of SiO2 162 13.1.2 LTO Process 164 13.1.3 PECVD Process of Silicon Dioxide 166 13.1.4 TEOS + 03 Deposition Using APCVD System 167 13.2 The Growth of Silicon Nitride Film 168 13.2.1 LPCVD 168 13.2.2 PECVD Process of Silicon Nitride 171 13.3 Atomic Layer Deposition Technique 174 14.1 Wet Etching 179 14.2 RIE System for Dry Etching 182 14.2.1 RIE Process Flow and Equipment Structure 182 14.2.2 Process Chamber 184 14.2.3 Vacuum Pumps 186 14.2.4 RF Power Supply (Source) and Matching Network (Matchwork) 187 14.2.5 Gas Cylinder and Mass Flow Controller (MFC) 189 14.2.6 Heater and Coolant 194	Lecture			

주별 강의내용						
주별	수업목표	수업내용	수업방식	자료, 과제 및 기타 참고사항	수업방식별시간	
					온라인	오프라인
11주	15 Dry Etching	15.1 The Etch Profile of RIE 197 15.1.1 Case 1 198 15.1.2 Case 2 201 15.2 Etching Rate of RIE 203 15.3 Dry Etching of III-V Semiconductors and Metals 206 15.4 Etch Profile Control 207 15.4.1 Influence of the PR Opening Shape on the Etch Profile 208 15.4.2 The Effect of Carbon on Etching Rate and Profile 209 15.5 Other Issues 211 15.5.1 The Differences Between RIE and PECVD 211 15.5.2 The Difference Between Si and SiO2 Dry Etching 214 15.6 Inductively Coupled Plasma (ICP) Technique and Bosch Process 215 15.6.1 Inductively Coupled Plasma Technique 216 15.6.2 Bosch Process 219	Lecture			
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15주	Final Examination	Written	Written Examination			